

CLAIMS

What is claimed is:

1. A central processing unit (CPU) that includes multiple clock zones, said CPU comprising:
 - in each clock zone,
 - at least one sensor that generates a signal indicative of a power supply voltage within said clock zone;
 - a clock generator for providing a variable frequency clock to said clock zone;
 - a first controller for controlling a frequency of operation of said clock generator in response to said at least one sensor, wherein said first controller further controls said frequency of operation in response to communication of frequency adjustments from first controllers in other clock zones within one cycle of latency; and
 - a second controller that provides an overdrive signal, that is combined with adjustment signals from said first controller for said clock generator, in response to communication of frequency adjustments from other clock zones beyond one cycle of latency.
2. The CPU of claim 1, wherein said clock generator only implements limited clock adjustments per clock cycle.
3. The CPU of claim 2, wherein each local zone further comprises: logic that determines an amount of clock adjustment of said clock generator that is unused by said first controller.
4. The CPU of claim 1 wherein each local zone comprises:
 - frequency mismatch logic for maintaining record of frequency mismatch between said clock zone and other clock zones; and
 - phase mismatch logic for maintaining record of phase mismatch between said clock zone and other clock zones.

5. The CPU of claim 4 wherein said second controller applies a larger frequency adjustment when phase mismatch recorded by said phase mismatch logic exceeds a threshold value.

6. The CPU of claim 1 further comprising:
a master phase-locked loop that generates a master clock, wherein each clock generator generates said variable clock frequency according to a clock period that is adjusted by a fraction of a period of said master clock.

7. The CPU of claim 1 wherein each local zone further includes:
a filter for filtering communication of frequency adjustments from other clock zones beyond one cycle of latency to account for concurrent frequency adjustments performed by said first controller in said local zone.

8. A method for operating a central processing unit (CPU) that includes multiple clock zones, said method comprising:
generating a respective variable frequency clock for each clock zone;
operating a sensor in each clock zone to generate a signal indicative of a power supply voltage within each respective clock zone;
adjusting, by a first controller, said respective variable frequency clock in each clock zone in response to said signal generated by said sensor;
adjusting, by said first controller, said respective variable frequency clock in each clock zone in response to communication of frequency adjustments in other clock zones within one cycle of latency; and
adjusting, by a second controller, said respective variable frequency clock by generating an overdrive signal, that is combined with adjustment signals from said first clock controller, in response to communication of frequency adjustments from other clock zones beyond one cycle of latency.

9. The method of claim 8, wherein each variable frequency clock may only be adjusted by a limited number of discrete adjustments per clock cycle.

10. The method of claim 9 further comprising:
determining a respective amount of clock adjustment capacity of each variable frequency clock that is unused by said respective first controller.

11. The method of claim 8 further comprising:
maintaining a record of frequency mismatch between each respective clock zone and other clock zones; and
maintaining a record of phase mismatch between each respective clock zone and other clock zones.

12. The method of claim 11 wherein each second controller applies a larger frequency adjustment when recorded phase mismatch exceeds a threshold value.

13. The method of claim 9 further comprising:
generating a master clock, wherein each variable clock frequency is varied by applying adjustments according to a fraction of a period of said master clock.

14. The method of claim 8 further comprising:
filtering, within each clock zone, communication of frequency adjustments from other clock zones beyond one cycle of latency to account for concurrent frequency adjustments performed by each respective first controller in said respective clock zone.

15. A central processing unit (CPU) that includes multiple clock zones, said CPU comprising:

in each clock zone,

at least one sensor means for generating a signal indicative of a power supply voltage within said clock zone;

clock means for providing a variable frequency clock to said clock zone;

first controller means for controlling a frequency of operation of said clock means in response to said at least one sensor means, wherein said first controller means further controls said frequency of operation in response to communication of frequency adjustments from first controllers means in other clock zones within one cycle of latency; and

second controller for generating an overdrive signal, that is combined with adjustment signals from said first controller means for said clock means, in response to communication of frequency adjustments from other clock zones beyond one cycle of latency.

16. The CPU of claim 15, wherein said clock means only implements limited clock adjustments per clock cycle

17. The CPU of claim 16, wherein each local zone further comprises: logic means for determining an amount of clock adjustment of said clock means that is unused by said first controller means.

18. The CPU of claim 15 wherein each local zone comprises: frequency mismatch means for maintaining record of frequency mismatch between said clock zone and other clock zones; and phase mismatch means for maintaining record of phase mismatch between said clock zone and other clock zones.

19. The CPU of claim 18 wherein said second controller means applies a larger frequency adjustment when phase mismatch recorded by said phase mismatch means exceeds a threshold value.

20. The CPU of claim 15, wherein each clock zone further comprises:
means for filtering communication of frequency adjustments from other clock zones beyond one cycle of latency to account for concurrent frequency adjustments performed by said first controller in said respective clock zone.